



TIBER 1CC-S MICROPROCESSOR

Tiber 1CC-S is an advance 32 bit embedded synthesizable processor, designed using 180nm to 90nm CMOS technology optimized for cache-less operations. The embedded processor is based on a high performance low power, advanced RISC CPU core. It is ideally suited for applications requiring a small footprint, low power consumption, and high performance.

Applications

- Cellular Phone
- Portable devices
- Bluetooth
- 32 bit microcontroller
- MP3 player
- Wireless module
- Digital Still Camera

Performance

- 180-225 MHz clock frequency
- <0.8 mW/Mhz
- Typical size 1.7 mm²
- Available in 180nm to 90nm

Features

- 32/16 bit RISC Architecture
 - supports v5te ISA
- Advanced Six-stage pipeline
- 16 Bit Code Compression
- Fast 32x32 MAC instructions
- Enhanced DSP Instructions
 - DSP Multiplies
 - DSP Saturating QADD & QSUB
- Optimized Load Latency
- Fast interrupt handler
- Fully static design
- Separate Instruction Interface
- Separate Data Interface
- Embedded JTAG ICE
- Streamlined Co-processor Interface

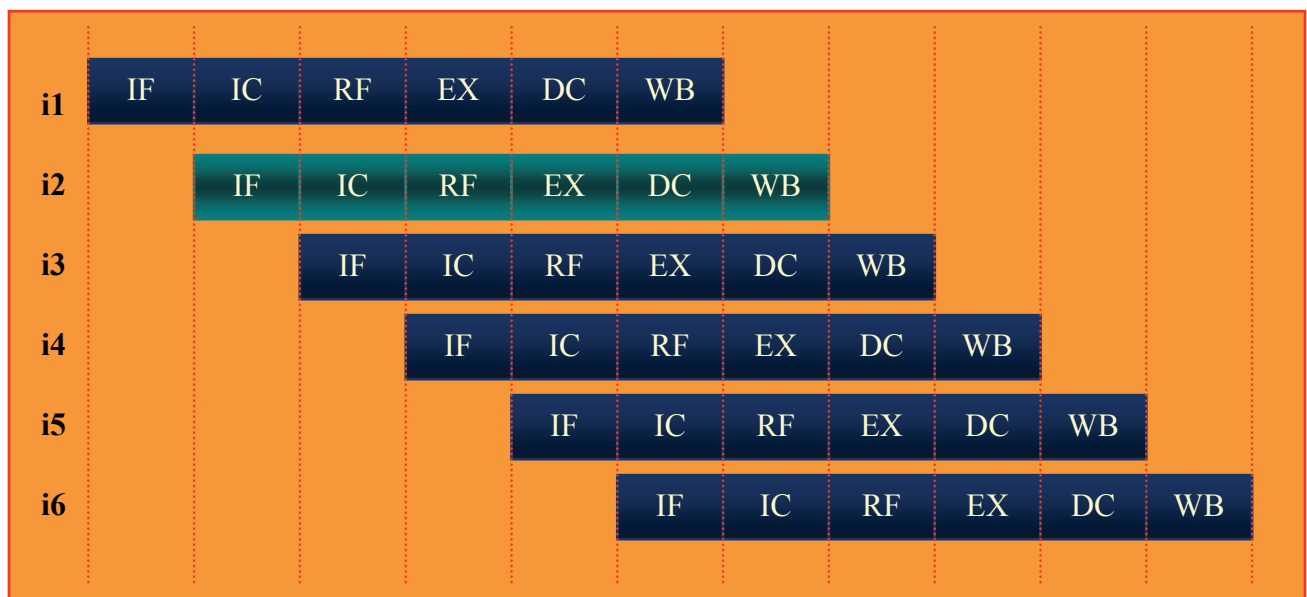


FIGURE 1: TIBER 1CC-S 6-Stage Pipeline

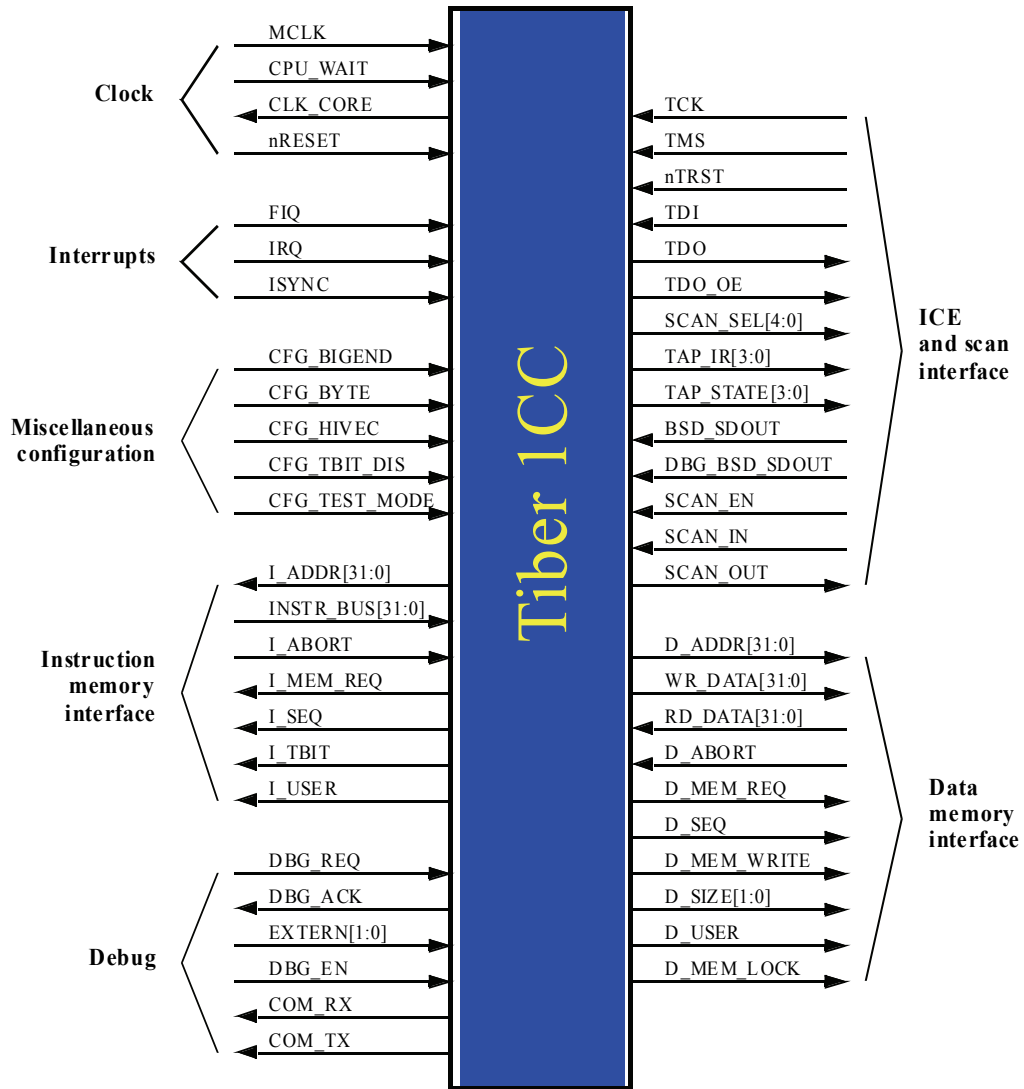


FIGURE 1: TIBER 1CC-S Block Interface

TOOLS

- Extensive SDK Support
- Include support for SDK from
 - Avalent
 - Sophia
 - YDC
 - Lauterbach
- Tiber development board
- SDK target C-model

SUPPORT

- Training
- Design consulting and design support

DELIVERABLES

- GDSII Data in specified technology and foundry or GTECH file for Synthesizable core.
- Synthesis Scripts for Design Compiler
- Encrypted RTL Simulation Model
 - Synopsys VCS
 - Cadence Verilog XL/NC Verilog
 - Mentor Graphicc ModelSim
- Test vectors
- ATPG vectors
- User manual
- Tiber development software tool kit
- Tiber development board
- AMBA AHB Interface RTL

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