

Janus 2CC is an advance 32 bit embedded processor, designed using 0.18 CMOS technology optimized for cache-less operations. The embedded processor is based on a high performance low power, advanced RISC CPU core. It is ideally suited for applications requiring a small footprint, low power consumption, and high performance.

Applications

- Cellular Phone
- Portable devices
- Bluetooth
- 32 bit microcontroller
- MP3 player
- Wireless module
- Digital Still Camera

Features

- 32/16 bit RISC Architecture
- Four-stage pipeline
- 16 Bit Code Compression
- Fast 32x32 MAC instructions
- Optimized Load Latency
- Fast interrupt handler
- Fully static design
- JTAG based debug capability

Performance

- 200 MHz clock frequency
- <0.25 mW/Mhz
- Typical size 1.1mm²
- Technology
 - 0.18um TSMC
 - 0.18um UMC

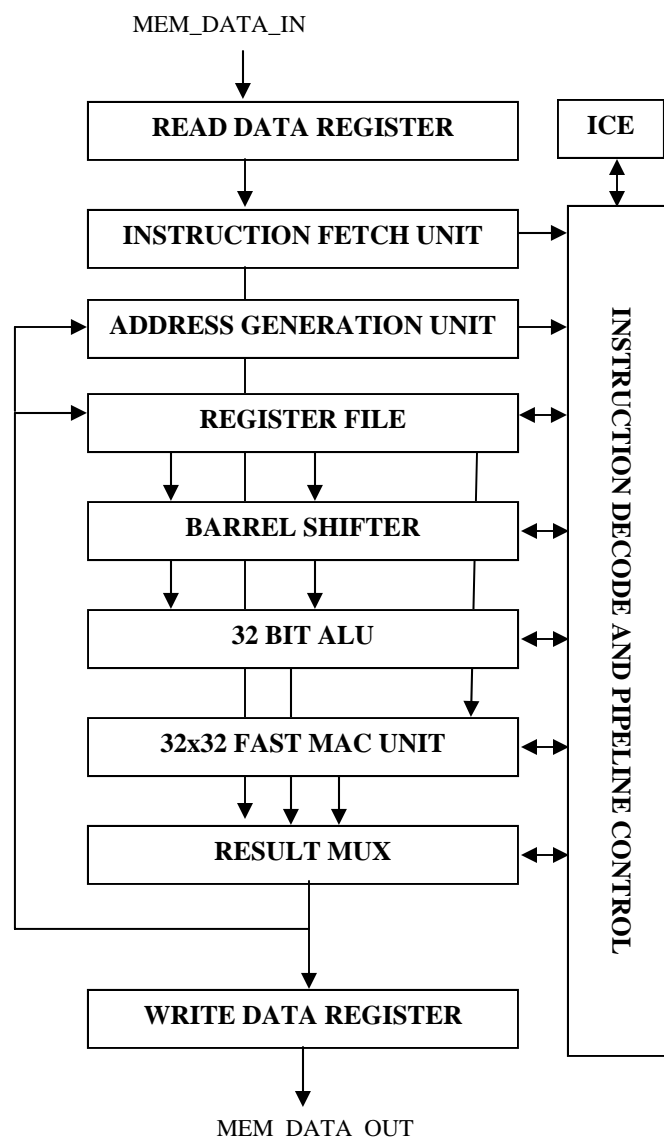


FIGURE 1: JANUS 2CC Core diagram

TOOLS

- Extensive SDK Support
- Include support for SDK from
 - Avalent
 - Sophia
 - YDC
 - Lauterbach
- Janus development board
- SDK target C-model

SUPPORT

- Training
- Design consulting and design support

DELIVERABLES

- GDSII Data in specified technology and foundry
- Encrypted RTL Simulation Model
 - Synopsys VCS
 - Cadence Verilog XL/NC Verilog
 - Mentor Graphicc ModelSim
- Test vectors
- ATPG vectors
- User manual
- Janus development software tool kit
- Janus development board
- AMBA AHB Interface RTL
- AMBA AHB-Lite Interface RTL

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