



# JANUS 220 MICROPROCESSOR CORE

Janus 220 is an advance 32 bit embedded processor core combining the Janus 2cc core with:

- 8KB unified Low Power Cache
- AMBA AHB Interface
- 32 Entry v4 compliant MMU
- 8 Entry Write Buffer

The on-chip unified cache and the write buffer, substantially raise the average execution speed and reduce the average amount of memory bandwidth required by the processor

## Applications

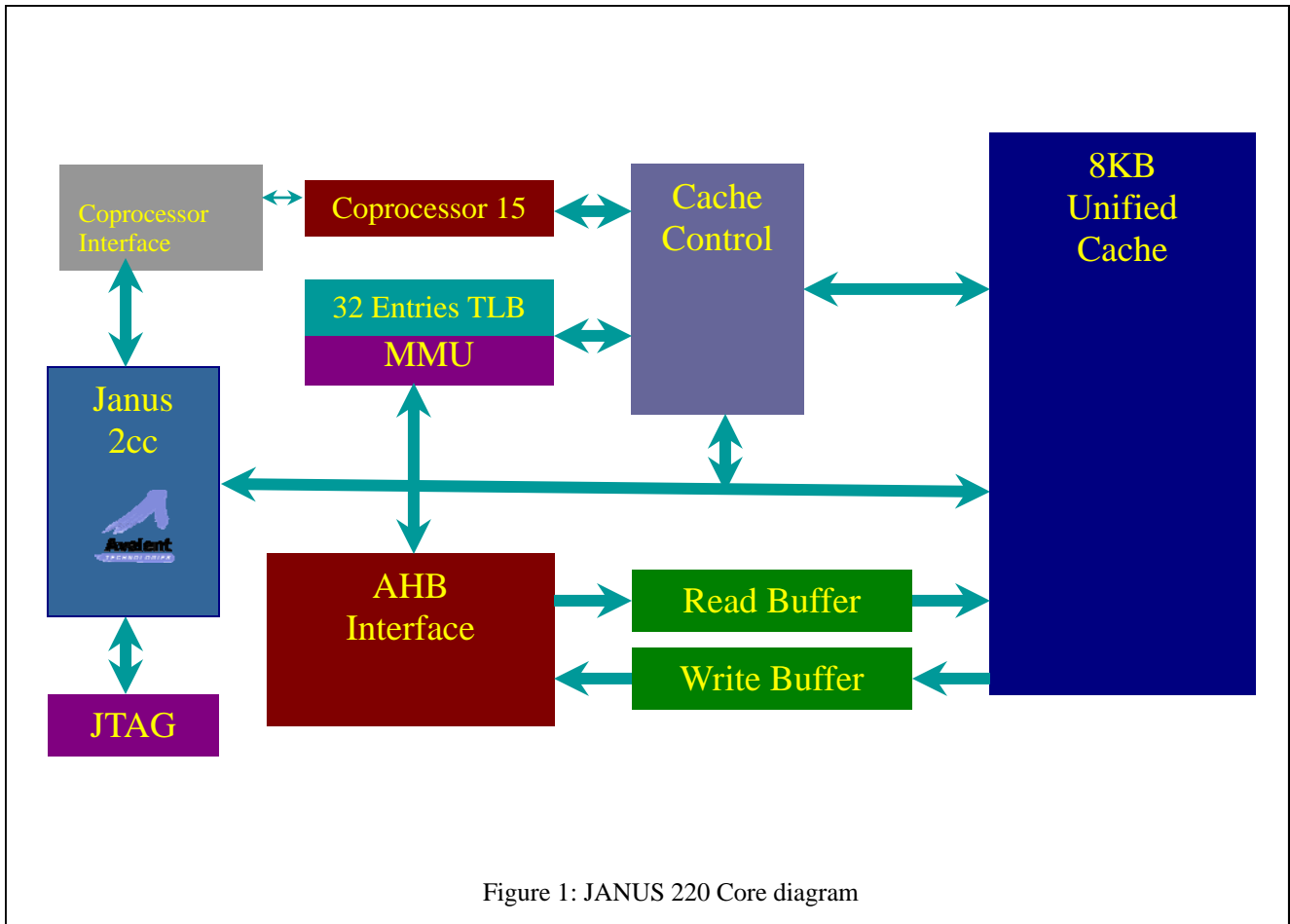
- Applications running an open OS
  - uClinux
- Internet Appliances
- Portable Media Players
- Networking Devices
- Digital Set-Top Box
- Embedded control applications
- XDSL and Cable Modems
- Residential gateways and routers
- Automotive control solutions
- 32 bit microcontroller
- MP3 player
- High Performance Wireless applications

## Performance

- 200 MHz clock frequency
- <0.53 mW/Mhz
- Typical size 3.0 mm<sup>2</sup>
- Technology
  - 0.18um TSMC
  - 0.18um UMC

## Features

- 32/16 bit RISC Architecture
- Four-stage pipeline
- 16 Bit Code Compression
- Fast 32x32 MAC instructions
- Optimized Load Latency
- Fast interrupt handler
- Programmable Cacheable/Bufferable regions
- 8KB unified power saving cache
  - 4-Way Set Associative
  - Random Replacement Algorithm
  - Cache Locking on per way basis for real time operations
  - Write-through cache policy
- Enhanced v4 compatible MMU
  - 32 TLB Entries
  - Hardware Page Table walker
  - 4k and 64K page size
  - 1M section size
  - protection scheme using domain and access features
  - separate access permission for section and pages.
  - 16 domains implemented in hardware
- 8 Entry write buffer to prevent the processor from stalling when writes to external memory are performed
- AMBA AHB Interface
- Memory BIST, and Scan
- Fully static design
- JTAG based debug capability



**TOOLS**

- Extensive SDK Support
- Include support for SDK from
  - Avalent
  - Sophia
  - YDC
  - Lauterbach
- Janus development board
- SDK target C-model

**SUPPORT**

- Training
- Design consulting and design support

**DELIVERABLES**

- GDSII Data in specified technology and foundry
- Encrypted RTL Simulation Model
  - Synopsys VCS
  - Cadence Verilog XL/NC Verilog
  - Mentor Graphicc ModelSim
- Test vectors
- ATPG vectors
- User manual
- Janus development software tool kit
- Janus development board

---

## **CONTACTING AVALENT**

---

### **UNITED STATE OF AMERICA**

Avalent Technologies Inc.  
405 River Oaks Parkway  
San Jose, CA 95148

Tel: +1-408-435-1188

Fax: +1-408-435-1511

Email: [info@avalent.com](mailto:info@avalent.com)

### **JAPAN**

Avalent Technologies Inc.  
Japan

Email: [japansales@avalent.com](mailto:japansales@avalent.com)